IN THE CLAIMS

Please cancel claims 1-20, and 44-46 without prejudice or disclaimer of the subject matter thereof.

Claims 1-20 (canceled)

21. (original) A semiconductor device in which plural wiring layers are formed over a semiconductor substrate and an active elements and an inductor are formed over the semiconductor substrate,

wherein the inductor is formed to the uppermost wiring layer among the plural wiring layers.

22. (original) A semiconductor device according to claim 21, wherein a bonding pad is formed to the device forming surface of the semiconductor substrate and the bonding pad is formed to the uppermost wiring layer.

23. (original) A semiconductor device according to claim 21, wherein the thickness of the uppermost wiring layer is greater than the thickness of the lower wiring layer formed below the uppermost wiring layer.

24. (original) A semiconductor device according to claim 21, wherein a capacitor element having a lower electrode and an upper electrode is formed over

the semiconductor substrate and the inductor is formed above the upper electrode of the capacitor element.

25. (original) A semiconductor device according to claim 24, wherein the lower electrode and the upper electrode of the capacitor element are formed of a metal film.

26. (original) A semiconductor device according to claim 21, wherein the device has plural stages of circuits operating at a frequency of 800 MHz or higher and the inductor forms an inter-stage matching circuit between the circuits.

27. (original) A semiconductor device according to claim 21, wherein the inductor has first and second terminals, the first terminal is formed in the uppermost wiring layer and the second terminal is formed in the lower wiring layer below the uppermost wiring layer.

28. (original) A semiconductor device in which the first wiring layer and a second wiring layer above the first wiring layer are formed over a semiconductor substrate, and a first capacitor element having a first lower electrode and a first upper electrode, and a second capacitor element having a second lower electrode and a second upper electrode are formed over the semiconductor substrate,

wherein the first lower electrode and the second lower electrode are formed, respectively, to the first wiring layer and the second wiring layer,

wherein a first circuit operating in a first frequency band and a second circuit operating in a second frequency band are formed over the semiconductor substrate,

wherein the first capacitor element is included in the first circuit and the second capacitor element is included in the second circuit, and

wherein the frequency included in the first frequency band is lower than the frequency included in the second frequency band.

29. (original) A semiconductor device according to claim 28, wherein the first frequency band includes 100 MHz and the second frequency band includes 800 MHz to 900 MHz or 1.8 GHz to 1.9 GHz.

30. (original) A semiconductor device according to claim 29, wherein the first lower electrode and the first upper electrode comprise silicon as a main ingredient and the second lower electrode and the second upper electrode comprise a metal as a main ingredient.

31. (original) A semiconductor device according to claim 29, wherein the second circuit is formed with plural stages of circuits and the second capacitor element forms an inter-stage matching circuit between plural stages of circuits in the second circuit.

32. (original) A semiconductor device comprising, over a semiconductor substrate:

a MISFET formed of source, drain, and gate electrode;

a resistor element;

a first capacitor element formed of a first lower electrode and a first upper electrode;

a second capacitor element formed of a second lower electrode and a second upper electrode; and

an inductor,

wherein a first silicon layer and a second silicon layer disposed over the first silicon layer are formed over the semiconductor substrate,

wherein a first metal layer, a second metal layer disposed over the first metal layer and a third metal layer disposed over the second metal layer are formed over the semiconductor substrate,

wherein the first silicon layer forms the first lower electrode of the first capacitor element and the resistor element,

wherein the second silicon layer forms the first upper electrode of the first capacitor element and the gate electrode of the MISFET, and

wherein the first metal layer forms the second lower electrode of the second capacitor element, the second metal layer forms the second upper electrode of the second capacitor element, and the third metal layer forms the inductor.

33. (original) A semiconductor device in which a passive element having two terminals is formed over the main surface of a semiconductor substrate, a conductive film is formed to the rear face of the semiconductor substrate, the

conductive film is connected with a fixed potential and one of the terminals of the passive element is electrically connected with the conductive film.

34. (original) A semiconductor device according to claim 33, wherein the passive element includes one or more of resistor element, capacitor element, and inductor.

35. (original) A semiconductor device according to claim 33, wherein the fixed potential is a ground potential.

36. (original) A semiconductor device according to claim 33, wherein an impurity layer is formed by introduction of impurities in the semiconductor substrate and one of the terminals of the passive element and the conductive film are electrically connected by way of the impurity layer.

37. (original) A semiconductor device according to claim 33, wherein a MISFET having gate and drain disposed to the main surface of the semiconductor substrate and a source disposed to the rear face of the semiconductor substrate is formed, and the source of the MISFET is electrically connected with the conductive film.

38. (original) A semiconductor device comprising: a well formed to the main surface of the semiconductor substrate; and a first MISFET having source,

drain, and gate disposed in the well over the main surface of the semiconductor substrate,

wherein the conductive film is formed to the rear face of the semiconductor substrate, the conductive film is connected with a fixed potential, and the well is electrically connected with the conductive film.

39. (original) A semiconductor device according to claim 38, wherein a second MISFET having gate and drain disposed to the main surface of the semiconductor substrate and the source disposed to the rear face of the semiconductor substrate is formed, and the source of the second MISFET is electrically connected with the conductive film.

40. (original) A semiconductor device according to claim 38, wherein the well has a p-conduction type and the fixed potential is a ground potential.

41. (original) A semiconductor device according to claim 38, wherein an impurity layer is formed by introduction of impurities in the semiconductor substrate, and the well and the conductive film are electrically connected by way of the impurity layer.

42. (original) A semiconductor device comprising: a well formed to the main surface of a semiconductor substrate; a first MISFET having, in the well, a source, a drain and a gate disposed to the main surface of the semiconductor

substrate; a second MISFET having gate and drain disposed to the main surface of the semiconductor substrate and a source disposed to the rear face of the semiconductor substrate; a passive element formed over the main surface of the semiconductor substrate and having two terminals; and a conductive film formed to the rear face of the semiconductor substrate,

wherein the conductive film is connected with a fixed potential, and one of the terminals of the passive element, the well, and the source of the second MISFET are electrically connected with the connective film.

43. (original) A semiconductor device comprising: a first circuit block and a second circuit block formed over a semiconductor substrate; and a conductive film formed to the rear face of the semiconductor substrate and connected with a ground potential,

wherein the first circuit block and the second circuit block include one of a circuit amplifying high frequency power or a circuit controlling the circuit block amplifying high frequency power, each of the first circuit block and the second circuit block has an impurity layer formed by introduction of impurities, and the first circuit block and the second circuit block are electrically connected by way of the impurity layer with the conductive film.

Claims 44-46 (canceled)